wherein the second bumps are formed of a metal which has a melting point lower than the melting point of the first bumps.

Please add new claim 33 as follows:

--33. The semiconductor device as defined in claim 1,

wherein there is a space between each of the conductive posts and an inner surface of each of the holes.--

REMARKS

Claims 1-33 are pending. By this Amendment, claims 1, 3, 7, 10 and 13 are amended, and claim 33 is added. No new matter is added. In view of the amendments presented above and the remarks presented below, Applicant respectfully requests that the objections and rejections in the Office Action be reconsidered and withdrawn.

The attached Appendix includes marked-up copies of each rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).

Although the Office Action indicates that claims 20-32 have already been withdrawn from further consideration, Applicant respectfully traverse the August 13 Restriction Requirement in Applicant's Response to Restriction Requirement filed on September 12.

Appreciation is respectfully expressed to the courtesy extended to Applicant's representative by Examiner Tran and Primary Examiner Tran during the July 23, 2002 personal interview.

Applicant gratefully acknowledges the indication in the Office Action that claims 7-9 and 13-15 would be allowable if rewritten to overcome the rejections under 35 U.S.C. §112, second paragraph. Applicant amends claims 7 and 13 into independent form to include all of the features of the base claims and any intervening claims. Thus, Applicant submits that these claims are in a condition for allowance.

The Office Action rejects claims 7-9 and 13-15 under 35 U.S.C. §112, second paragraph, as being indefinite. Applicant, however, respectfully traverses the rejections of claims 7-9 and 13-15.

Regarding claim 7, Applicant respectfully submits that the scope of "a recognition hole is formed ... including the interconnecting pattern," recited in claim 7, is clear to a person of ordinary skill in the art when taken in light of the specification. See, for example, the specification starting in line 1 of page 25 and Fig. 6, which describes in a non-limiting and exemplary manner the recognition hole 50 and the recognition pattern 52.

Regarding claim 13, Applicant respectfully submits that "the melting point" has inherent antecedent basis as being an inherent characteristic of any material.

Regarding claim 18, Applicant respectfully submits that "the semiconductor device" has antecedent basis in the recitation "[a] semiconductor device," as recited in claims 1-6, from which claim 18 depends.

In light of the above, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. §112, second paragraph, rejections of claims 7-9 and 13-15.

The Office Action rejects claims 1-5, 10, 11, and 17 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,949,142 to Otsuka; and rejects claims 6, 12, 16, 18, and 19 under 35 U.S.C. §103 as being obvious over Otsuka. These rejections are respectfully traversed.

In particular, Applicant asserts that Otsuka does not disclose or suggest a semiconductor device, including at least conductive posts provided on the electrodes and within the holes to be electrically connected to the interconnecting pattern, as recited in independent claim 1.

Although Otsuka discloses conductive bumps 4c, the conductive bumps 4c are not provided on the electrodes of the chip 2. Moreover, the conductive bumps 2a are not provided within holes. Thus, Applicant asserts that claims 1-6, 10-12 and 16-19 define patentable subject matter.

In view of the above, Applicant respectfully requests that the rejection of claims 1-6, 10-12 and 16-19 be reconsidered and withdrawn.

In view of the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance. Applicant, therefore, earnestly solicits favorable consideration and prompt allowance of this application.

Should the Examiner believe that anything further is desirable in order to place this application in better condition for allowance, the Examiner is requested to contact the Applicant's attorney at the telephone number listed below.

Respectfully submitted,

James A. Oliff
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JAO:RSE

Attachment:
Appendix

Date: September 18, 2002

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

APPENDIX

Changes to Claims:

The following are marked-up versions of the amended claims:

1. (Amended) A semiconductor device comprising:

a substrate including a plurality of holes and a surface over which an interconnecting pattern is formed, part of the interconnecting pattern being superposed over the holes;

a semiconductor chip disposed over another surface of the substrate and including a plurality of electrodes to be positioned over the holes; and

conductive ~~members~~ posts provided on the electrodes and within the holes ~~for~~ to be electrically ~~connecting the electrodes~~connected to the interconnecting pattern.

3. (Amended) The semiconductor device as defined in claim 2,

wherein the resin is an anisotropic conductive material containing conductive particles; and

wherein the conductive ~~members~~ posts are electrically connected to the interconnecting pattern through the conductive particles.

7. (Twice Amended) ~~The semiconductor device as defined in claim 1,~~ A semiconductor device comprising:

a substrate including a plurality of holes and a surface over which an interconnecting pattern is formed, part of the interconnecting pattern being superposed over the holes;

a semiconductor chip disposed over another surface of the substrate and including a plurality of electrodes to be positioned over the holes; and

conductive members provided within the holes for electrically connecting the electrodes to the interconnecting pattern,

wherein a recognition hole is formed in the substrate at a position differing from the holes; and

wherein a recognition pattern is formed over the recognition hole on the side of a surface of the substrate including the interconnecting pattern.

10. (Twice Amended) The semiconductor device as defined in claim 1, wherein the conductive ~~members~~ posts are a plurality of layered bumps.

13. (Amended) ~~The semiconductor device as defined in claim 11,~~ A semiconductor device comprising:

a substrate including a plurality of holes and a surface over which an interconnecting pattern is formed, part of the interconnecting pattern being superposed over the holes;

a semiconductor chip disposed over another surface of the substrate and including a plurality of electrodes to be positioned over the holes; and

conductive members provided within the holes for electrically connecting the electrodes to the interconnecting pattern,

wherein the conductive members are a plurality of layered bumps,

wherein the bumps include first bumps formed on the electrodes and second bumps formed on the first bumps,

wherein the second bumps are formed of a metal which has a melting point lower than the melting point of the first bumps.